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EXAMINER	
LEWIS, DAVID LEE	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/182,435	FUJIOKA ET AL.	
	Examiner	Art Unit	
	David L Lewis	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-12 and 19-30* is/are allowed.

6)☒ Claim(s) *1-8,13,15,16 and 18* is/are rejected.

7)☐ Claim(s) *14 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11; 5/23/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 9-12 previously allowed, claims 19-30 allowed over the prior art of record.

Claim Objections

2. Claims 14 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. **Claims 1, 3, and 5 are rejected under 35 U.S.C. 102(a) as being anticipated by Tsuchi et al. (5,818,406).**

5. **As in claim 1, Tsuchi et al. teaches of** a liquid crystal display device comprising: a liquid crystal display panel, **figure 2**; and for supplying a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel, **figure 2 item 5**; said picture signal line driving circuit having a switching circuit in which a first transistor, to whose gate electrode a control voltage is applied, **figure 1 item 3**, and a second transistor to whose gate electrode a bias voltage is applied are connected in series, **figure 1 item 1**. **As in claim 3,** Tsuchi et al. teaches wherein the first and the second transistors are first conducting type transistors, and a second conducting type transistor is connected to the first transistor in parallel, figure 1 and 6b.

6. **As in claim 5, Tsuchi et al. teaches of** a liquid crystal display device, comprising a liquid crystal display panel and a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel, **column 4 lines 40-67**; said picture signal line driving circuit further including: a first input terminal, **figure 1 item Vnd**, a second input terminal, **figure 1 item Vpd**, and a common output terminal, **figure 1 item 5**, a first switching element connected between the first input terminal and the common output terminal, **figure 1 item** 1 and 3, and a second switching element connected between the second input terminal and the common output terminal, figure 1 item 2 and 4 , the first and second switching elements including a transistor at a input port, to whose gate electrode a control voltage is applied connected in series with a transistor at a output port, to whose gate electrode a bias voltage is applied, figure 1 items Vng, Vpg, 3, and 4, column 8 lines 23-35, figure 5, 9, and 10 .

7. **Claims 1 and 13 are rejected under 35 U.S.C. 102(a) as being anticipated by Kubota et al. (5,754155).**

8. **As in claim 1, Kubota et al. teaches of** a liquid crystal display device comprising: a liquid crystal display panel, **figure 1**; and for supplying a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel, **figure 1 item 1**; said picture signal line driving circuit having a switching circuit in which a first transistor, to whose gate electrode a control voltage is applied, **figure 17 item TR5a**, and a second transistor to whose gate electrode a bias voltage is applied are connected in series, **figure 17 item TR5b, Vb5a**.

9. **As in claim 13, Kubota et al teaches** of liquid crystal display device, **figure 1**, comprising: a liquid crystal display panel, **figure 1 item 1**; and a picture signal line driving circuit which applies a picture signal voltage to the liquid crystal display panel, the picture signal line driving circuit including a switching circuit, **figure 1 item 2**; wherein the switching circuit includes a first transistor having an input, an output, and a gate electrode, **figure 17 item TR5a**, the gate electrode of the first transistor having a control voltage applied thereto, the control voltage being effective for turning the first transistor on and off, **figure 17 item IN**, and a second transistor having an input, an output, and a gate electrode, **figure 17 item TR5b**, the gate electrode of the second transistor having a bias voltage applied thereto, **figure 17 item Vb5a**, the input of the

second transistor being connected to the output of the first transistor so that the first transistor and the second transistor are connected in series, **figure 17 items TR5a and TR5b.**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 2, 4, 6, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchi et al. (5,818,406).**

11. **As in claims 2, 4, 6, and 8, Tsuchi et al is silent** as to said well bias formation, however **said features would have been obvious to the skilled artisan** at the time of the invention as a design choice given **Tsuchi teaches** of a first and second transistor of the same type, figure 1 items 1 and 3, and therefore obviously being tied to the same well layer construction as is well known, having a sufficient minimum bias allowing the device to function properly. **Tsuchi teaches** of an applied voltage bias, Vng, and while Tsuchi is silent as to said voltage bias being different from the well layer bias, it would

have also been obvious to the skilled artisan for said voltages to be different given there distinct functions within the scope of the transistor operation, there distinct separate implementation, Tsuchi makes no mention of them being tied to a common line, and no specific illustration of such a common value is shown. **As in claim 7,** said first and second conducting types and parallel formation would have been obvious to the skilled artisan as a design choice given Tsuchi teaches of alternative embodiments wherein said second conducting and parallel formation is shown in figure 6.

12. **Claims 15, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota et al. (5,754155).**

13. **As in claims 15, 16, and 18, Kubota et al is silent** as to said well bias formation, however **said features would have been obvious to the skilled artisan** at the time of the invention as a design choice given **Kubota teaches** of a first and second transistor of the same type, and therefore obviously being tied to the same well layer construction as is well known, having a sufficient minimum bias allowing the device to function properly. **Kubota teaches** of an applied voltage bias, Vb5, and while **Kubota** is silent as to said voltage bias being different from the well layer bias, it would have also been obvious to the skilled artisan for said voltages to be different given there distinct functions within the scope of the transistor operation, there distinct separate implementation, **Kubota** makes no mention of them being tied to a common line, and no specific illustration of such a common value is shown.

Response to Arguments

14. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection, further said arguments do not correspond to the prior art used to reject the claims. See the above Non-final rejection in view of Tsuchi et al. (5818406) or Kubota et al (5754155). Claims 9-12 and 19-30 are allowable over the prior art of record. Claims 14 and 17 are objected to. The Examiner apologizes for the long response delay and will accommodate any efforts by Applicant to speed up prosecution.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L Lewis whose telephone number is 703 306-3026. The examiner can normally be reached on M, T, TH, F. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-4700.

Any response to this action should be mailed to:
Commissioner of Patents and Trademarks

Washington, D.C. 20231
or faxed to:
(703) 872-9314 (for Technology Center 2600 only)
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

May 4, 2004

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600